WHAT IS CLAIMED IS:

1. A programmable integrated circuit including a memory block, the memory block comprising:

a plurality of address recycling multiplexers each having a first address input coupled to receive address signals, and a select input coupled to receive an address stall signal;

a plurality of address registers each having a data input coupled to an output of a corresponding one of the address recycling multiplexers, and an output coupled to a second input of the corresponding one of the address recycling multiplexers; and

an address decoder coupled to the outputs of the address registers.

2. The programmable integrated circuit of claim 1 wherein each of the address registers has a clock input coupled to receive a clock signal.

3. The programmable integrated circuit of claim 2 wherein the memory block further comprises:

a second plurality of multiplexers configurable to couple programmable interconnect lines to the address recycling multiplexers.

4. The programmable integrated circuit of claim 1 wherein the memory block further comprises:

an array of SRAM memory cells; and

data registers coupled to receive data signals and to transmit the data signals to the array of memory cells.

5. The programmable integrated circuit of claim 1 wherein the programmable integrated circuit is a field programmable gate array that is part of a system on a chip.

6. A method for storing address signals during a stall state of a cache memory, the method comprising:

providing address signals at first inputs of address recycling multiplexers;

coupling the first inputs of the address recycling multiplexers to data inputs of address registers when an address stall signal is in a first state;

providing the address signals to an address decoder;

providing decoded address signals from the address decoder to the cache memory; and

coupling output terminals of the address registers to second inputs of the address recycling multiplexers when the address signal is in a second state during a refresh of the cache memory.

7. The method of claim 6 wherein providing the address signals at the first inputs of the address recycling multiplexers further comprises:

coupling interconnect lines to the first inputs of the address recycling multiplexers through second multiplexers.

8. The method of claim 6 wherein providing the address signals to an address decoder further comprises:

transmitting each set of the address signals from the data inputs to the output terminals of the address registers in response to every other edge of a clock signal.

9. The method of claim 6 further comprising:

generating the address stall signal in a programmable logic block in response to a refresh of the cache memory.

10. The method of claim 6 further comprising:

providing data to the cache memory using data registers.

11. The method of claim 6 wherein the address multiplexer, the address registers, the address decoder and the cache memory all reside within a circuit block a programmable integrated circuit.

12. The method according to claim 11 wherein the programmable integrated circuit is part of a system on a chip.

13. A integrated circuit including a memory block, the memory block comprising:

an address decoder circuit block;

address registers coupled to inputs of the address decoder circuit block and coupled to receive a clock signal at clock inputs;

an address recycling block that causes the address registers to store address signals during multiple cycles of the clock signal when an address stall signal is in a first state,

wherein the address recycling block has first inputs coupled to receive the address signals, second inputs coupled to outputs of the address registers, a select input coupled to receive the address stall signal, and outputs coupled to data inputs of the address registers.

14. The integrated circuit as defined in claim 13 wherein the address recycling block includes a plurality of multiplexers coupled in parallel between the first and second inputs and the outputs of the address recycling block.

15. The integrated circuit as defined in claim 13 wherein the address signals are coupled to the first inputs of the address recycling block through programmable multiplexers and driver circuits.

16. The integrated circuit as defined in claim 13 wherein the integrated circuit is a field programmable gate array, and the address stall signal is generated by a programmable logic block.

17. The integrated circuit as defined in claim 16 wherein field programmable gate array is part of a system that includes a processor and a memory unit.

18. The integrated circuit as defined in claim 13 wherein the integrated circuit operates the memory block as a cache memory.

19. The integrated circuit as defined in claim 13 wherein the memory block includes an array of SRAM memory cells, and the address decoder circuit block selects word lines in the SRAM array.